CLAIMS

We claim:

1. A mixer circuit for reducing the power level of spurious output signals, the mixer comprising:

a first mixer stage which includes a mixer with first and second input ports and an a first output port;

a second mixer stage which includes a second mixer with third and forth input ports and a second output port, said first input port electrically coupled to one or the other of said third and fourth input ports;

a phase modulator for phase modulating a first local oscillator signal, said phase modulator electrically coupled to one or the other of said first and second input ports; and

an inverse phase modulator for inverse phase modulating a second local oscillator signal, said inverse phase modulator electrically coupled to the other of said third and fourth input ports.

2. The mixer circuit as recited in claim 1, wherein said phase modulator is a phase shift keying (PSK) modulator.

3. The mixer circuit as recited in claim 2, wherein said inverse phase modulator is a phase shift keying (PSK) modulator.

4. The mixer circuit as recited in claim 2, wherein said phase modulator is a first direct sequence binary phase shift keying (BPSK) modulator modulated according to a psuedorandom number (PN) code and said mixer circuit includes a PN code generator for generating said PN code.

5. The mixer circuit as recited in claim 4, wherein said inverse phase modulator is a second direct sequence binary phase shift keying modulator modulated according to said PN code.

6. The mixer circuit as recited in claim 1, further including an intermediate filter coupled between said first output port and one of said third and fourth input ports.

7. A mixer circuit for reducing the power levels of spurious output signals comprising:

a first mixer having first and second input ports and a first output port; and

a phase modulator for phase modulating a first local oscillator signal, said phase modulator electrically coupled to one or the other of said first and second input ports.

8. The mixer circuit as recited in claim 7, further including a second mixer having third and fourth input ports and a second output port, said first output port electrically connected to one or the other of said third and fourth input ports.

9. The mixer circuit as recited in claim 8, further including an inverse phase modulator, electrically coupled to the other of said third and fourth input ports, said inverse phase modulator configured to inverse phase modulate a second local oscillator signal.

10. The mixer circuit as recited in claim 9, wherein said phase modulator is a direct sequence binary phase shift keying (BPSK) modulator and said mixer circuit includes a psuedorandom number (PN) code generator for generating a PN code for said direct sequence modulation.

11. The mixer circuit as recited in claim 10, wherein said inverse phase modulator is a direct sequence BPSK modulator modulated by said PN code from said PN code sequence generator.

12. The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for QPSK modulation.

13. The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for PSK modulation.

14. The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for M-ary modulation techniques.

15. The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for GMSK modulation techniques.

16. A mixer circuit for reducing the power levels of spurious output signals comprising:

a first mixer having first and second input ports and a second output port; and

first means for phase modulating a first local oscillator signal applied to one or the other of the first and second input ports.

17. The mixer circuit as recited in claim 16, further including a second mixer circuit having third and forth input ports and a second output port, said first output port connected to one or the other of said third and fourth input ports.

18. The mixer circuit as recited in claim 17, further including second means for phase modulating a second local oscillator signal applied to the other of said third and fourth input ports.

19. The mixer circuit as recited in claim 18, wherein said second phase modulating means is an inverse phase modulator.

20. The mixer circuit as recited in claim 19, wherein said first phase modulating means includes a first phase shift keying (PSK) modulator.

21. The mixer circuit as recited in claim 20, wherein said first PSK modulator is a direct sequence binary PSK (BPSK) modulator and said phase modulating means includes a psuedorandom number (PN) code sequence generator for generating a PN code for modulating said local oscillator signal.

22. The mixer circuit as recited in claim 21, wherein said inverse phase modulator is a direct sequence binary phase shift (BPSK) modulator modulated according to the same PN code as said first means.

23. The mixer as recited in claim 16, wherein said first means includes a first modulation source and the system further includes an inverse modulator for inverse modulating the modulation source.

24. The mixer as recited in claim 18, wherein said first means and second means are configured for QPSK modulation.

25. The mixer as recited in claim 18, wherein said first means and second means are configured for PSK modulation.

26. The mixer as recited in claim 18, wherein said first means and second means are configured for M-ary modulation.

27. The mixer as recited in claim 18, wherein first means and second means are configured for GMSK modulation.

28. A method of reducing the power levels of spurious output signals at the output of a mixer circuit comprising the steps of:

(a) providing a two stage mixer including first and second mixer each having a local oscillator port, an input port for receiving first and second local oscillator signals;

(b) phase modulating the first local oscillator signal; and

(c) inverse phase modulating the second local oscillator signal.

29. The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by BPSK modulation techniques.

30. The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by QPSK modulation techniques.

31. The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by GMSK modulation techniques.

32. The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by M-ary modulation techniques.